

Figure 1 is a block diagram of a processor architecture, labeled 100. The architecture is divided into several main functional units:

- Instruction Fetch Unit (101):** This unit contains:
 - IFAR (102):** Instruction Fetch Address Register.
 - Branch Target Address Cache (105):** Receives branch targets and provides them to the IFAR.
 - Instruction Cache (103):** Provides instructions to the Branch Scan Logic.
 - Branch Prediction Logic Unit (104):** A central unit containing:
 - GHV Mechanism (106):** Receives branch information from the Branch Scan Logic and provides feedback to the Branch Target Address Cache.
 - BMTs (107):** Branch Mispredicted Targets.
 - Count Cache (108):** Tracks branch counts.
 - Link Stacks (109):** Stores return addresses for branches.
 - Branch Scan Logic (110):** Receives instructions from the Instruction Cache and provides branch information to the Branch Prediction Logic Unit and the Branch Info Queue.
 - Branch Info Queue (111):** Stores branch information and provides it to the Branch Prediction Logic Unit and the Instruction Sequencer Unit.
- Instruction Decode Unit (112):** Receives instructions from the Branch Prediction Logic Unit and provides them to the Instruction Sequencer Unit.
- Instruction Sequencer Unit (113):** Receives instructions from the Instruction Decode Unit and provides dispatched instructions to the execution units.
- Execution Units:** Dispatched instructions are sent to:
 - Load/Store Unit (114):** Handles load and store instructions.
 - Fixed Point Unit (115):** Handles fixed-point arithmetic.
 - Floating Point Unit (116):** Handles floating-point arithmetic.
 - Branch Execution Unit (117):** Receives branch information from the Branch Prediction Logic Unit and the Branch Info Queue, and provides feedback to the Branch Prediction Logic Unit.

The diagram illustrates the flow of instructions and branch information through the processor, highlighting the role of the Branch Prediction Logic Unit in managing branch targets and mispredictions.

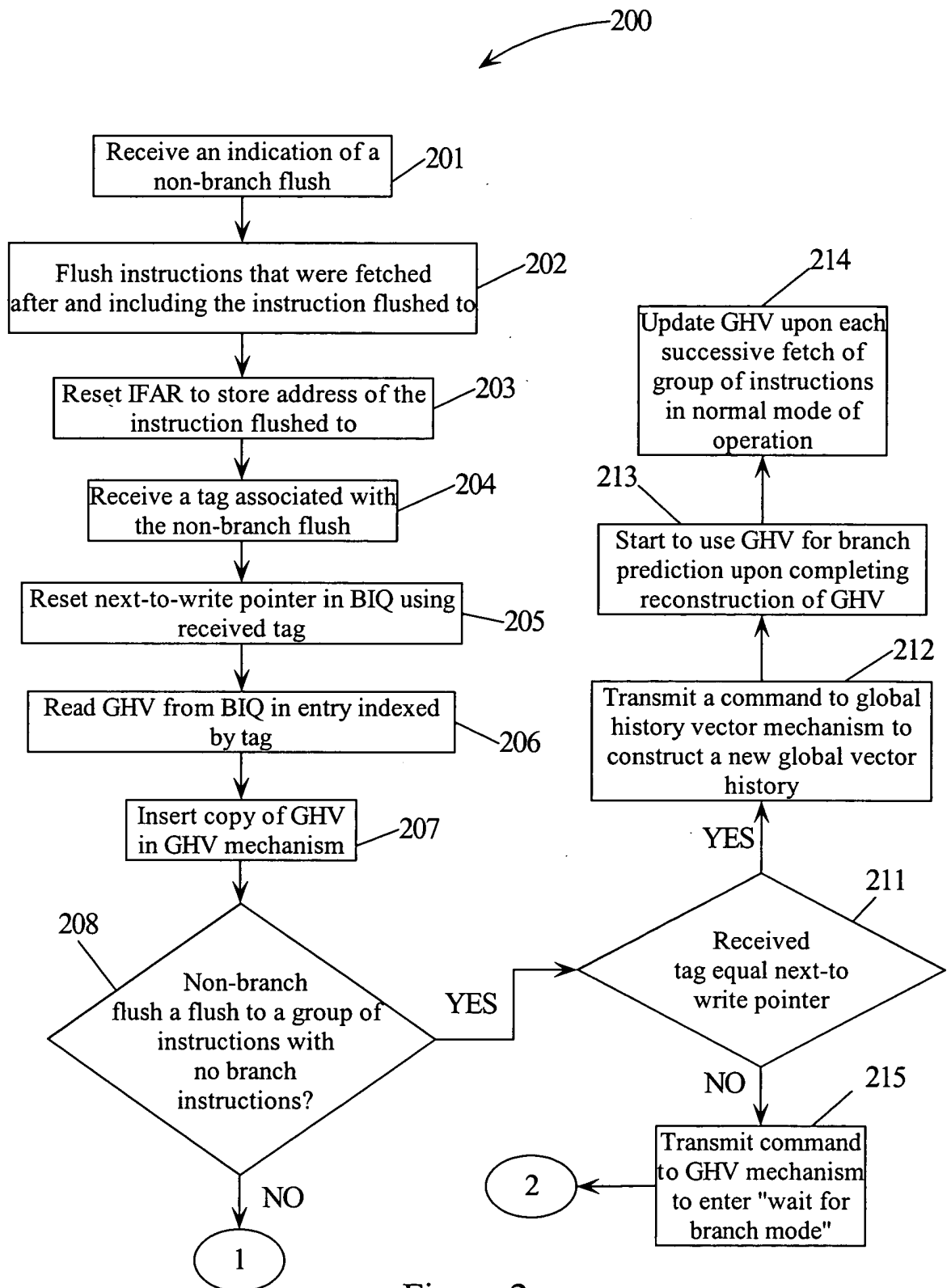


Figure 2

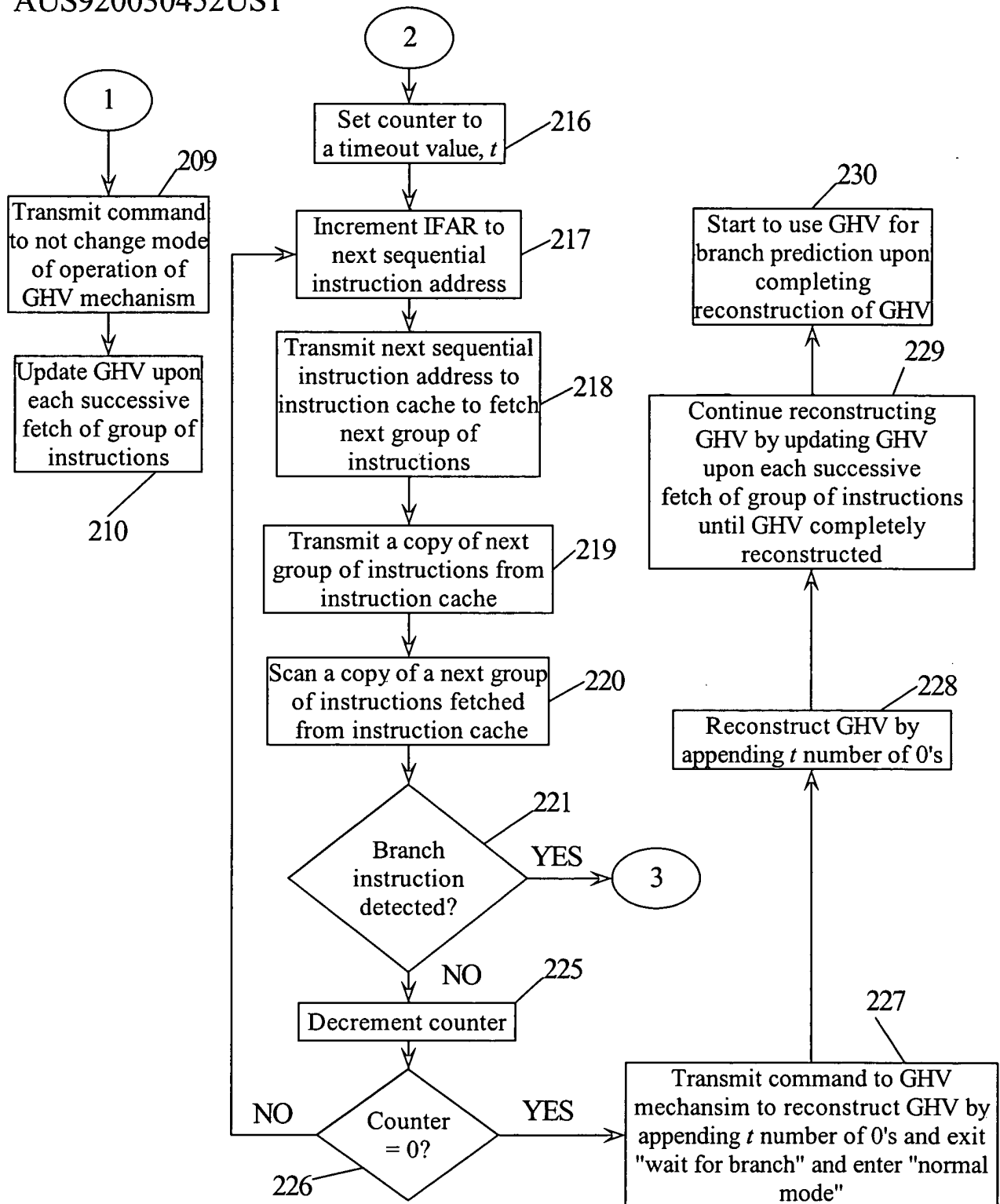


Figure 2 (continued)

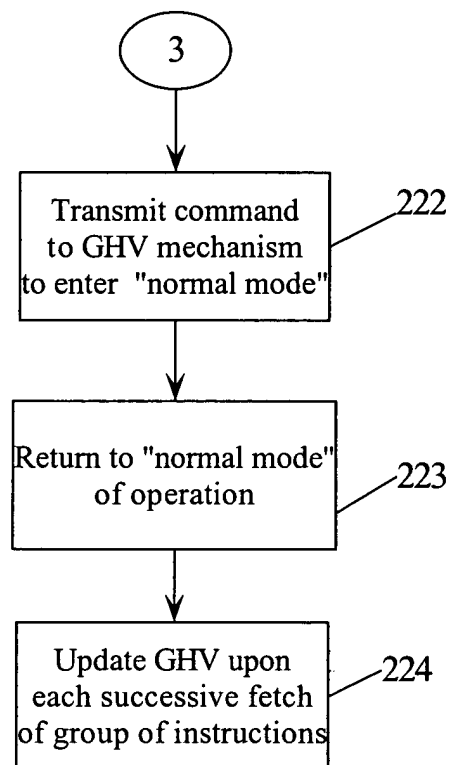


Figure 2 (continued)

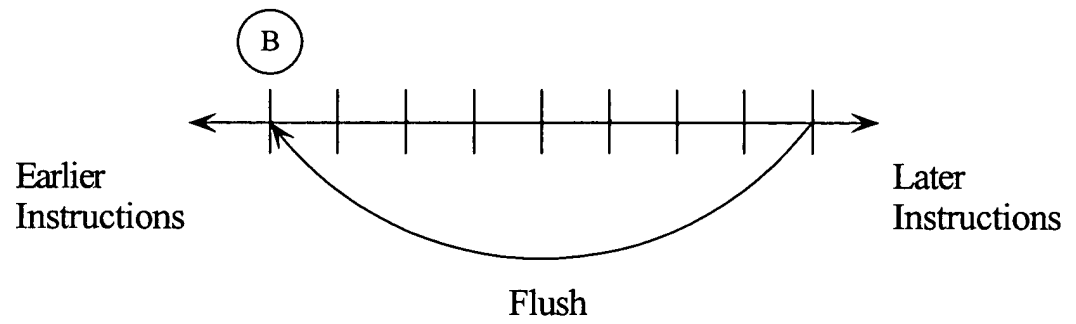


Figure 3

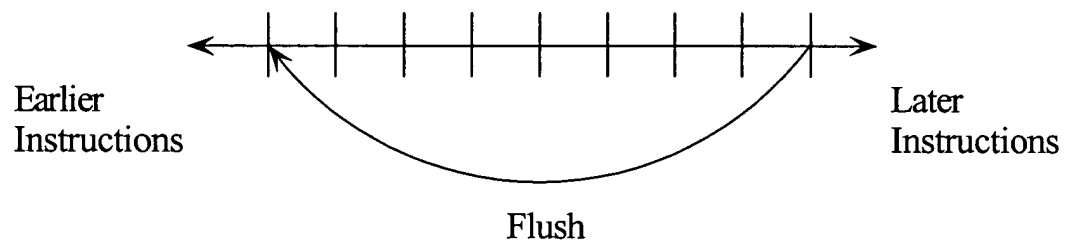


Figure 4

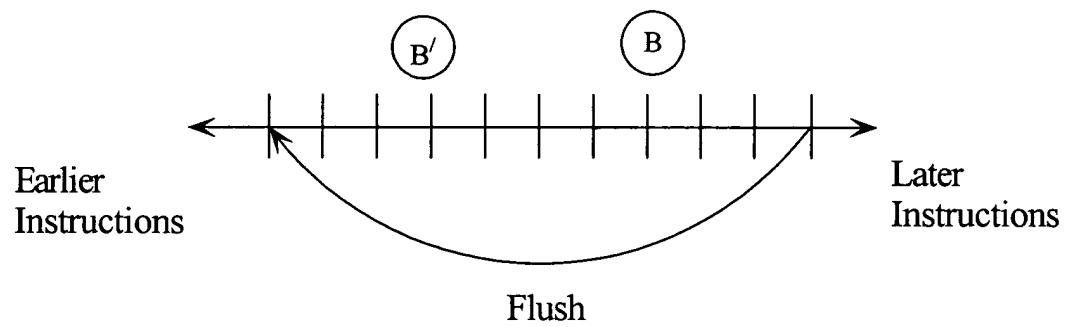


Figure 5